CLMPTO
CLAIMS 1-8 (CANCELLED)

9. A method of forming a semiconductor device, comprising:

forming an NMOS transistor and a PMOS transistor having respective gates each comprising a polysilicon portion and a silicide portion, wherein channel regions of the NMOS transistor and the PMOS transistor comprise strained silicon;

forming a metal layer in contact with the silicide portion of the NMOS gate while protecting the PMOS gate; and

annealing to fully silicide the NMOS gate.

10. The method claimed in claim 9, wherein, after annealing, the gate of the NMOS transistor has a work function that exceeds a work function of the gate of the PMOS transistor so as to compensate for a difference in respective threshold voltages of the NMOS transistor and the PMOS transistor caused by the strained silicon of the channel regions.

11. The method claimed in claim 10, wherein the difference of the work functions of the NMOS and PMOS gates is approximately the same as the difference of the threshold voltages of the NMOS and PMOS transistors.

12. The method claimed in claim 9, wherein forming a metal layer in contact with the silicide portion of the NMOS gate while protecting the PMOS gate comprises:

forming a conformal protective layer over the NMOS transistor and the PMOS transistor;

forming a silicon oxide layer over the protective layer;

planarizing the silicon oxide layer to exposed portions of the protective layer above the respective gates;

masking the PMOS transistor;

CLAIMS 13-22 (CANCELLED)